PRODUCT BRIEF

Pigeon Point BMR-A2F-VPX Reference Design

Board Management Reference Design for VPX and ANSI/VITA 46.11-2022

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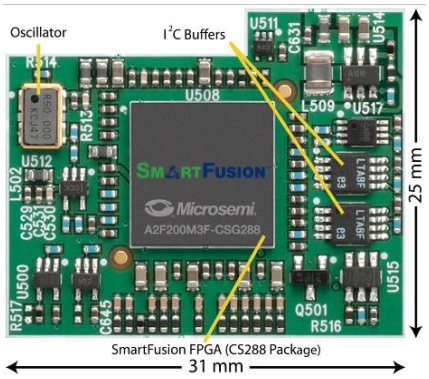
The BMR-A2F-VPX design is one of a series of Pigeon Point Board Management Reference designs. This member of the series provides a Tier-2 or Tier-1 Intelligent Platform Management Controller (IPMC) for VPX and VITA 46.11-2022 and is based on the SmartFusion intelligent mixed-signal FPGA from Microsemi Corporation.

This reference design is delivered in a Pigeon Point Board Management Starter Kit (which is detailed in a separate Product Brief). The kit includes:

- A SmartFusion FPGA design that implements the core of a VITA 46.11-2022 Tier-2 or Tier-1 IPMC, working with the Cortex-M3 ARM processor and supporting peripherals in the microcontroller subsystem (MSS). This design is ready to be adapted for your VPX plug-in module or other intelligent Field Replaceable Unit (FRU), such as a fan tray.
- Schematics for a corresponding IPMC subsystem, ready for integration into the schematic for your board, with adaptation as necessary
- Firmware for that subsystem, delivered in source form and with development tools—ready for simple and quick adaptation to your requirements
- Derived from widely used BMR-A2F-ATCA product, inheriting substantial benefits from more than a decade of field use and interoperability testing for BMR-based management controllers
- One-stop support from nVent for schematics, firmware and software used in developing and delivering your Pigeon Point BMR-based IPMC
- Complementary support from Microsemi for the FPGA design, including adaptations to meet the specific needs of your board

The photo in the next column shows the core of a BMR-A2F-VPX IPMC. The active components are:

- The A2F200 intelligent mixed-signal FPGA.
- Dual IPMB buffers to isolate the IPMC from dual redundant System IPMB implemented on the backplane.
- An external oscillator to provide the operating frequency.



ANSI/VITA 46.11-2022 Tier-1 and Tier-2 IPMC

- The BMR-A2F-VPX based Tier-2 or Tier-1 IPMC complies with ANSI/VITA 46.11-2022, System Management on VPX
- PICMG HPM.1 R1.0, the Firmware Upgrade specification
- HPM.2 and HPM.3, the LAN-attached IPM Controller and DHCP-assigned Platform Management Parameters specifications (revisions R1.1 and R2.0, respectively)
- IPMI v1.5, document revision 1.1 and the relevant subset of IPMI v2.0, document revision 1.0, plus relevant errata
- HPM.2/3 and IPMI 2.0 compliance includes support for Internet Protocol version 6 (IPv6)[1]
- Benefits from thorough testing in ATCA context with other management components at PICMG TCA-IWs (Interoperability Workshops) VPX-specific VSO event

Full support for core hardware requirements

- 32-bit Cortex-M3 operating at 80 MHz for IPMC firmware execution
- VITA 46.11- and IPMI-aware monitoring of designated SmartFusion analog sensors via SmartFusion's programmable analog subsystem, without using Cortex-M3 processor cycles
- Supports A2F200/500 variants, including CS288, FG256 and FG484 packages

[1] IPv6 support is not present in ANSI/VITA 46.11; it was added to the ATCA HPM subsystem after VITA 46.11 was modeled on that subsystem. Any future IPv6 support in VITA 46.11 will likely be modeled on the ATCA support, as well.

- Payload voltage monitoring (including the various power supply rails that can be delivered from a VPX backplane)
- Thermal sensors (internal SmartFusion temperature monitors with external bipolar transistors and/or external DS75 digital sensors)
- HPM.2-compatible direct LAN attachment interface or sideband LAN attachment interface implemented via either non-proprietary Network Controller Sideband Interface (NC-SI) or Intel-proprietary SMBus sideband interface to payload NCs, capable of handling IPMI over LAN (including Serial over LAN, HPM.1 upgrades, IPMB trace access and other HPM.2-compliant extensions)
- Dual redundant System IPMB, with VITA 46.11-compliant option to use just IPMB-A, without IPMB-B
- System IPMB supports Fast-Mode (i.e. 400 kHz) operation
- Geographic address detection from backplane
- FRU LED management
- Payload power supply controls (multiple voltage levels), with optional persistence across IPMC resets
- Optional local System Event Log (SEL)
- Optional infrastructure for non-intelligent Rear Transition Modules
- UART- or LPC/KCS-based payload interface
- UART-based serial debug interface

Small footprint

- Core IPMC can fit in the following package-dependent footprints: 25mm x 31mm (CS288), 29.5mm x 34mm (FG256) or 34mm x 44mm (FG484)

Optional support for special purpose functionality

- Telco (dry contact) alarm management
- Chassis FRU Information SEEPROM access

Programmable analog subsystem eliminates Cortex-M3 processor cycles for monitoring analog sensors

- Within Analog Compute Engine, Sample Sequencing Engine (SEE) monitors up to 32 SmartFusion analog inputs, with Post Processing Engine (PPE) configurable to do IPMI-compatible processing of the readings, including threshold detection
- Only readings that cross thresholds result in interrupts to the Cortex-M3 processor
- Fully configurable sensor sampling and threshold details, using Microsemi MSS Configurator tool

Instance-specific information storage in SmartFusion FlashROM

- Optional support in firmware for retrieving instance-specific information (such as a module serial number) from special 1 Kbit FlashROM area that can only be written via JTAG
- Coordinates with Microsemi tool facilities to allow automatic serializing of successively programmed SmartFusion devices

Adaptable and extendable FPGA design

- Initial FPGA design provided in several variants (e.g. for different package sizes), can be used directly or modified
- Potential modifications include adding or removing Microsemi IP blocks, adding custom logic and/or IP blocks, changing device pin assignments, if necessary

Comprehensive, readily adaptable firmware

- All mandatory and many optional IPMI/VPX commands supported over System IPMB
- Numerous Pigeon Point extension commands, primarily used over the payload and serial debug interfaces
- Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands
- PICMG HPM.1 firmware upgrade support
- Simple—but highly flexible—configuration of firmware features

Sophisticated, HPM.1-compliant support for firmware upgrades

- Firmware upgrades over any IPMI interface to the IPMC, with redundant copies and automatic fallback after failed upgrade
- IPMC is fully functional during upgrade
- Bootloader can be upgraded without using JTAG
- Framework for managing firmware upgrades that include changes in data structures that are preserved across IPMC resets to eliminate disruptive upgrades
- IPMC FRU Information implemented as additional HPM.1 component, allowing FRU Information upgrades independently of firmware
- Optional capability to upgrade FPGA design without using JTAG
- Optional upgrades via IPMI over LAN interface
- Open source ipmitool supplied as upgrade agent
- HPM.1 compliance means that any compliant upgrade agent can upgrade any compliant IPMC

Optional support for non-intelligent Rear Transition Modules (RTM)

- Includes specific hardware and firmware support for interface between front board and RTM
- Allows compliance with VITA 46.11 requirements regarding how an RTM is represented by the IPMC

Choice of serial interface protocols (SIPL variants) supported via UARTs to payload processor and serial debug interface

- SIPL-TM, based on IPMI-defined Terminal Mode of the Serial/Modem Interface,
- SIPL-BM based on IPMI-defined Basic Mode,
- Either protocol selectable individually for either serial interface
- SIPL-TM: human-oriented and ASCII-based, intended primarily for the serial debug interface
- SIPL-BM: machine-oriented and binary-based, intended primarily for the UART-based payload interface
- Both protocols use encoded forms of raw IPMI messages, which are handled by the IPMC essentially like IPMB messages

Optional use of LPC/KCS for payload interface[2]

- Enabled in lieu of UART-based payload interface
- Based on IPMI-defined KCS variant of IPMI System Interface, implemented over LPC in Microsemi CoreLPC
- Facilitates use of existing IPMI software on payload processor, which often interfaces with management controller via KCS

Optional Simple Network Stack

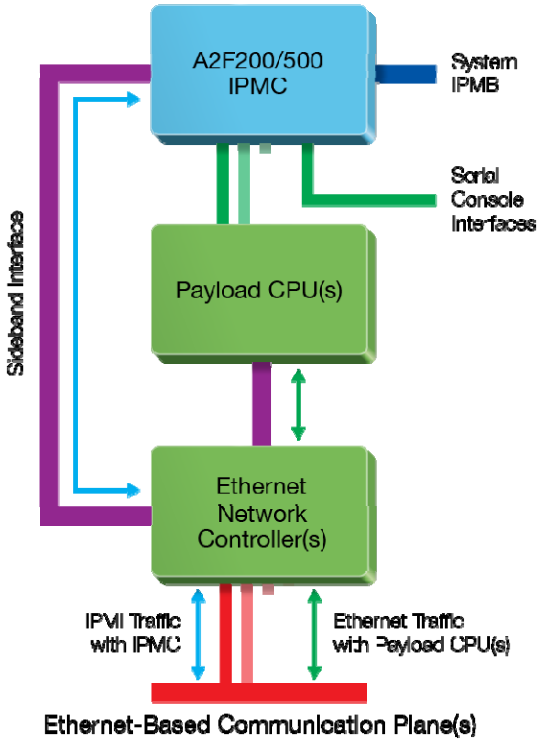
- Ethernet layer, including drivers for SmartFusion Ethernet MAC and for SMBus sideband link to selected Intel NCs
- Internet Protocol (IP) layer, which cooperates with ARP module to resolve IP address to MAC addresses
- IP-based protocol layer, including UDP and ICMP
- Provides foundation for application protocols, such as RMCP and RMCP+

Optional HPM.2 IPMI over LAN

- Primary client of simple network stack
- IPMI 2.0 compliant implementation of extended Remote Management Control Protocol (RMCP+), including session establishment
- RMCP+ compliant authentication, integrity and confidentiality, specifically via the following algorithms (all using IPMI 2.0-compliant random number generation):
  - Authentication: HMAC-SHA1
  - Integrity: HMAC-SHA1-96
  - Confidentiality**:** AES-CBC-128
- IPMI over LAN and SoL payload types in RMCP+, with framework for supporting further payload types
- Enables HPM.1 firmware upgrades and HPM.2 IPMI trace collection via LAN channel
- Optional HPM.3 IPv4 or IPv6 parameter assignment via direct interaction with DHCPv4

[2] LPC/KCS implements the IPMI-defined Keyboard Controller Style interface using the Low Pin Count version of the Peripheral Component Interconnect (PCI) bus that is used for access to low speed peripherals such as management controllers.

or DHCPv6 server or by Shelf Manager[3] or other proxy
- Supported LAN interfaces with SmartFusion RMII-equipped Ethernet MAC include:
  - NC-SI[4], tested with selected Intel NCs
  - UMP (Universal Management Port, a Broadcom predecessor to NC-SI), tested with Broadcom BCM5714C
  - Direct Ethernet, where the LAN connection is dedicated to management traffic, not shared with the payload
- Additional supported LAN interface with SMBus sideband interface: Intel-proprietary pass-through



Optional HPM.2 Serial over LAN (SoL)
- Uses HPM.2 IPMI over LAN facility to support Serial over LAN via NC-SI, UMP, or Intel-proprietary pass-through on SMBus or a direct Ethernet connection
  - Payload SoL requires separate physical UART connection between payload and IPMC
  - SoL for IPMC serial debug interface available, also
  - HPM.2 SOL extensions allow up to 15 concurrent SOL sessions, each with specific serial ports accessible to the IPMC, user chosen from up to 255 physical on-board serial ports
- Supplied open source ipmitool can be used as SoL client

Optional local System Event Log (SEL)
- Requires SEEPROM storage on board
- IPMI compliant System Event Log for events generated on the FRU(s) represented by the IPMC
- Can provide a useful historical record of events that have been recorded during operation of a board, perhaps for use in board diagnosis at a maintenance depot
- Events are also forwarded to Chassis Manager, as required by VITA 46.11

Optional support for persistent modifications to Sensor Data Records
- Non-volatile copy of SDR Repository can be configured in on-board SEEPROM
- Sensor threshold and hysteresis values can be configured dynamically via Pigeon Point extension commands, and are thereafter persistent across power cycles and resets of the board

Optional support for payload-controlled sensors
- Allows sensors that are implemented by the payload (e.g. an I^2C sensor connected to the payload CPU) but exposed by the IPMC as its own
- Covers discrete and threshold sensors

3 The Pigeon Point Shelf Manager can be configured to assign IPv4 address parameters to LAN-attached IPMCs via HPM.3-defined mechanisms.

4 NC-SI is an open specification published by the Distributed Management Task Force (DMTF, www.dmtf.org) that uses the Reduced Media Independent Interface (RMII) as the physical transport between the network and management controllers.

Optional support for persistent configuration parameters

- Parameters preserve values across IPMC power cycles and resets
- Used for most persistent data, such as serial port parameters, LAN and SoL parameters
- Framework for such treatment of other parameters, including those in custom firmware extensions

Simple, but powerful, firmware configuration mechanisms

- Configuration variables in a single config.h source file parameterize and determine inclusion/exclusion of subsystems during firmware image build
- Configuration data for programmable analog created in MSS Configurator, imported into BMR build
- Binary configuration files for FRU Information and Sensor Data Records (SDR) merged into firmware image
- FRU Information and SDR files produced from textual representations by special supplied compilers

Comprehensive Cortex-M3 development environment

- x86 Linux-based development environment included with BMR-A2F-VPX Starter Kit (based on Mentor Graphics Sourcery Code Bench G++ Lite toolchain)
- Windows-based development environment (the Microsemi SoftConsole Integrated Development Environment) available for download from Microsemi
- JTAG-based firmware download using Microsemi FlashPro3/4 JTAG programmer (FlashPro4 included with Starter Kit)

Numerous extensions beyond required IPMI/VITA 46.11/HPM.1 commands and functionality

- Warm Reset
- Get Device GUID
- Set BMC Global Enables
- Reset Watchdog Timer
- Set Watchdog Timer
- Get Watchdog Timer
- Get BMC Global Enables
- Clear Message Flags
- Get Message Flags
- Get Message
- Send Message
- Get System GUID
- Set User Name
- Get/Set Sensor Hysteresis
- Get/Set Sensor Thresholds
- Get/Set Sensor Event Enable
- Re-arm Sensor Events
- Get Sensor Event Status
- Get Sensor Type
- Activate/Deactivate Payload
- Suspend/Resume Payload Encryption
- Get Payload Activation Status
- Get Payload Instance Info
- Get/Set User Payload Access
- Get Channel Payload Support
- Get Channel Payload Version
- Get Channel OEM Payload Info Command
- Get/Set SOL Configuration Parameters
- FRU Control
  - Graceful Reboot and Issue Diagnostic Interrupt options
- Get FRU LED Properties
- Get LED Color Capabilities
- Get/Set FRU LED State
  - Lamp Test function
- Set FRU Activation
- Get FAN Speed Properties
- Get/Set Fan Level
- Get IPMB Link Info
- Get/Set FRU Persistent Control
- FRU Persistent Control Capabilities
- Get Power Supply Capabilities
- Get/Set Power Supply Status
- Abort Firmware Upgrade
- Query Self-test Results
- Query Rollback Status
- Initiate Manual Rollback

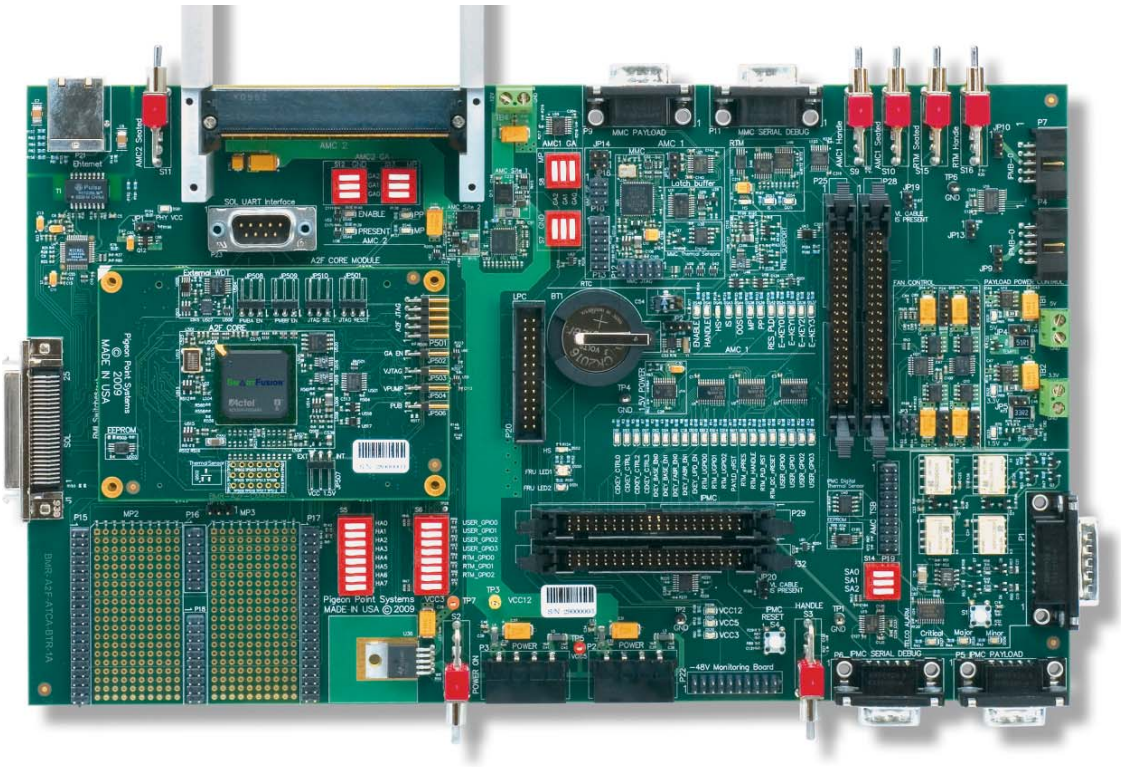
Rich set of Pigeon Point extension commands

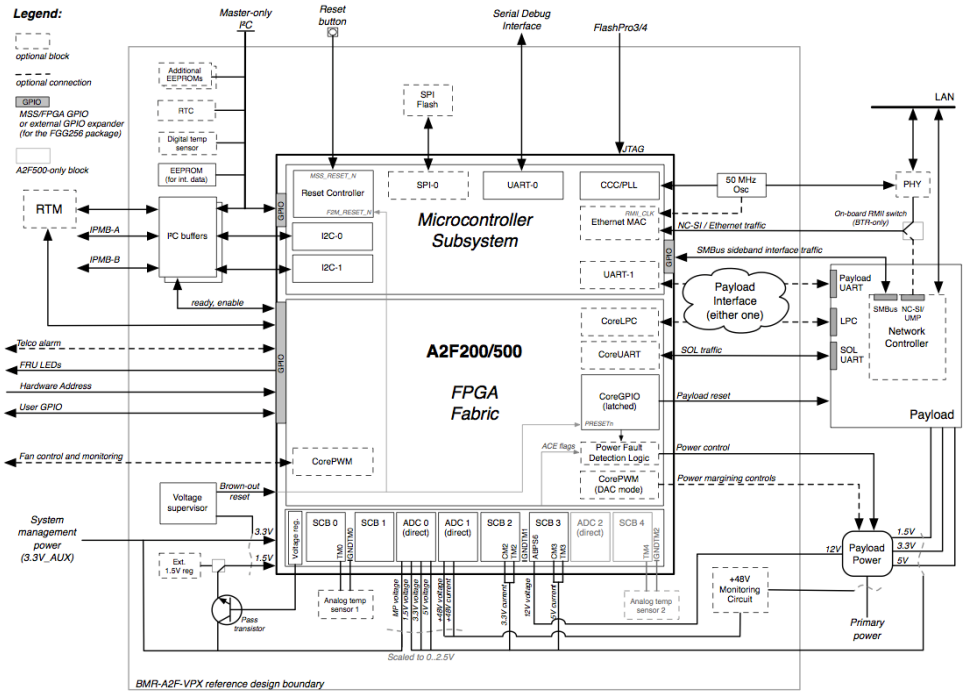
- All extension commands implemented as IPMI-compliant OEM messages
- Get Status
- Get/Set Serial Interface Properties
- Get/Set Debug Level
- Get/Set Hardware Address
- Get/Set Payload Communication Timeout
- Disable/Enable Payload Control
- Reset IPMC
- Hang IPMC[5]
- Graceful Reset
- Diagnostic Interrupt Results
- Set/Clear Telco Alarm
- Get Telco Alarm Sensor Number
- Get/Set Payload Shutdown Timeout
- Get/Set Local FRU LED State
- Update Discrete Sensor
- Update Threshold Sensor
- Set EEPROM SDR Data
- Set EEPROM SDR Hysteresis
- Set EEPROM SDR Thresholds
- Reset EEPROM SDR Repository
- Calibrate AFS Temperature Sensor
- Get/Set GPIO Signal State
- Reset Non-Volatile Parameters and Reboot
- Get FPGA Design Version
- Get/Set PWM DAC Level
- Get/Set FRU Info Write-Protect State

Reference Implementation

A bench top implementation called the BMR-A2F-IPMC-BTR is shown on the next page. In addition to the BMR-A2F-VPX core, the board includes implementations of optional IPMC features and numerous LEDs, switches and headers to allow lab experimentation with the behavior of the IPMC. This board is used also with BMR-A2F-ATCA solutions and contains components supporting those solutions that are not used in a VPX context. Below the photo is a block diagram of a BMR-A2F-VPX based IPMC.

[5] This function is used to test the IPMC watchdog.




Legend:
optional block
optional connection
GPIO
MSS/FPGA GPIO or external GPIO expander (for the FGG256 package)
A2F500-only block
Master-only I²C
Reset button
Serial Debug Interface
FlashPro3/4
JTAG
Additional EEPROMs
RTC
Digital temp sensor
EEPROM (for int. data)
SPI Flash
RTM
IPMB-A
IPMB-B
I²C buffers
ready, enable
Reset Controller
SPI-0
UART-0
CCC/PLL
50 MHz Osc
Microcontroller Subsystem
I2C-0
I2C-1
Ethernet MAC
UART-1
LAN
PHY
NC-SI / Ethernet traffic
On-board RMII switch (BTR-only)
SMBus sideband interface traffic
Payload Interface (either one)
Payload UART
LPC
SOL UART
SMBus
NC-SI/ UMP
Network Controller
Payload
A2F200/500
FPGA Fabric
CoreLPC
CoreUART
CoreGPIO (latched)
CorePWM
Telco alarm
FRU LEDs
Hardware Address
User GPIO
Fan control and monitoring
SOL traffic
Payload reset
Power control
Power margining controls
Power Fault Detection Logic
CorePWM (DAC mode)
Voltage supervisor
Brown-out reset
System management power (3.3V_AUX)
3.3V
1.5V
Ext. 1.5V reg
Pass transistor
SCB 0
SCB 1
ADC 0 (direct)
ADC 1 (direct)
SCB 2
SCB 3
ADC 2 (direct)
SCB 4
Analog temp sensor 1
Analog temp sensor 2
Scaled to 0..2.5V
+48V Monitoring Circuit
Payload Power
12V
1.5V
3.3V
5V
Primary power
BMR-A2F-VPX reference design boundary