PRODUCT BRIEF

Pigeon Point BMR-ZNQ-VPX IPMC Reference Design

Board Management Reference Design for VPX and ANSI/VITA 46.11-2022

May 13, 2022

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The BMR-ZNQ-VPX design is one of a series of Pigeon Point Board Management Reference designs. This member of the series provides a Tier-2 or Tier-1 Intelligent Platform Management Controller (IPMC) for VPX and VITA 46.11-2022 and is based on the Xilinx Zynq® UltraScale+™ device.

The BMR-ZNQ-VPX IPMC design provides a reference IPMC design integrated in with a customer VPX system based on the Xilinx Zynq® UltraScale+™ device.

This reference design is delivered in a Pigeon Point Board Management Starter Kit (which is detailed in a separate Product Brief). The kit includes:

- A reference design that implements the core of a VITA 46.11-2022 Tier-2 or Tier-1 IPMC, using only low-power domain (LPD) processor and peripherals of the Xilinx Zynq® UltraScale+™ deviceThis design is ready to be adapted for your VPX plug-in module or other intelligent Field Replaceable Unit (FRU), such as a fan tray.
- Firmware for that subsystem running on the real-time processing unit (RPU) of the Xilinx Zynq® UltraScale+™ device, delivered in source form—ready for simple and quick adaptation to your requirements
- One-stop support from nVent for schematics and firmware, and delivering your Pigeon Point BMR-based IPMC, with complementary support from Xilinx

ANSI/VITA 46.11-2022 Tier-1 and Tier-2 IPMC
- The BMR-ZNQ-VPX based Tier-2 or Tier-1 IPMC complies with ANSI/VITA 46.11-2022, System Management on VPX
- PICMG HPM.1 R1.0, the Firmware Upgrade specification
- HPM.2 and HPM.3, the LAN-attached IPM Controller and DHCP-assigned Platform Management Parameters specifications (revisions R1.1 and R2.0, respectively)
- IPMI v1.5, document revision 1.1 and the relevant subset of IPMI v2.0, document revision 1.0, plus relevant errata

- HPM.2/3 and IPMI 2.0 compliance includes support for Internet Protocol version 6 (IPv6)[1]

ANSI/VITA 46.11-2022 Tier-3 IPMC
With the purchase of the Pigeon Point Board Management Starter Kit Add-on (detailed in a separate product brief) customers are able to implement an ANSI/VITA 46.11-2022 compliant Tier-3 IPMC

Full support for core hardware requirements
- Cortex-R5-based Real-Time Processing Unit for IPMC firmware execution
- Monitoring of internal Zynq US+ Processing System (PS) rails using the System Monitoring block of the processor subsystem (SYSMON-PS)
- Payload voltage monitoring (including the various power supply rails that can be delivered from a VPX backplane) using the optional System Monitoring block in the Programmable Logic (SYSMON-PL)
- Thermal sensors
- HPM.2-compatible direct LAN attachment interface or sideband LAN attachment interface implemented via either non-proprietary Network Controller Sideband Interface (NC-SI) or Intel-proprietary SMBus sideband interface to payload NCs, capable of handling IPMI over LAN (including Serial over LAN, HPM.1 upgrades, IPMB trace access and other HPM.2-compliant extensions)
- Dual redundant System IPMB, with VITA 46.11-compliant option to use just IPMB-A, without IPMB-B
- System IPMB supports Fast-Mode (i.e. 400 kHz) operation
- Geographic address detection from backplane
- FRU LED management
- Payload power supply controls (multiple voltage levels) using PMBus or control GPIOs, with optional persistence across IPMC resets
- Optional local System Event Log (SEL)
- Optional infrastructure for non-intelligent Rear Transition Modules
- (Virtual) UART-based payload interface

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[1] IPv6 support is not present in ANSI/VITA 46.11; it was added to the ATCA HPM subsystem after VITA 46.11 was modeled on that subsystem. Any future IPv6 support in VITA 46.11 will likely be modeled on the ATCA support, as well.

- UART-based serial debug interface
- Virtual UART for communicating with the Xilinx Zynq® UltraScale+™ (can be used as a Payload or SoL interface)
- External SPI-based UART bridge

Optional support for special purpose functionality
- Chassis FRU Information SEEPROM access

Comprehensive, readily adaptable firmware
- All mandatory and many optional IPMI/VPX commands supported over System IPMB
- Numerous Pigeon Point extension commands, primarily used over the payload and serial debug interfaces
- Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands
- PICMG HPM.1 firmware upgrade support
- Simple—but highly flexible—configuration of firmware features

Sophisticated, HPM.1-compliant support for firmware upgrades
- Firmware upgrades over any IPMI interface to the IPMC, with redundant copies and automatic fallback after failed upgrade
- IPMC is fully functional during upgrade
- Bootloader can be upgraded without using JTAG
- IPMC FRU Information implemented as additional HPM.1 component, allowing FRU Information upgrades independently of firmware
- Optional capability to upgrade FPGA design without using JTAG
- Optional upgrades via IPMI over LAN interface
- Open source ipmitool supplied as upgrade agent
- HPM.1 compliance means that any compliant upgrade agent can upgrade any compliant IPMC

Optional support for non-intelligent Rear Transition Modules (RTM)
- Includes specific hardware and firmware support for interface between front board and RTM
- Allows compliance with VITA 46.11 requirements regarding how an RTM is represented by the IPMC

Choice of serial interface protocols (SIPL variants) supported via UARTs to payload processor and serial debug interface
- SIPL-TM, based on IPMI-defined Terminal Mode of the Serial/Modem Interface,
- SIPL-BM based on IPMI-defined Basic Mode,
- Either protocol selectable individually for either serial interface
- SIPL-TM: human-oriented and ASCII-based, intended primarily for the serial debug interface
- SIPL-BM: machine-oriented and binary-based, intended primarily for the UART-based payload interface
- Both protocols use encoded forms of raw IPMI messages, which are handled by the IPMC essentially like IPMB messages

Optional Simple Network Stack
- Ethernet layer, including driver for Xilinx Zynq® UltraScale+™ Ethernet MAC
- Internet Protocol (IP) layer, which cooperates with ARP module to resolve IP address to MAC addresses
- IP-based protocol layer, including UDP and ICMP
- Provides foundation for application protocols, such as RMCP and RMCP+

Optional HPM.2 IPMI over LAN
- Primary client of simple network stack
- IPMI 2.0 compliant implementation of extended Remote Management Control Protocol (RMCP+), including session establishment
- RMCP+ compliant authentication, integrity and confidentiality, specifically via the following algorithms (all using IPMI 2.0-compliant random number generation):
  - Authentication: HMAC-SHA1
  - Integrity: HMAC-SHA1-96
  - Confidentiality: AES-CBC-128
- IPMI over LAN and SoL payload types in RMCP+, with framework for supporting further payload types
- Enables HPM.1 firmware upgrades and HPM.2 IPMI trace collection via LAN channel
- Optional HPM.3 IPv4 or IPv6 parameter assignment via direct interaction with DHCPv4 or DHCPv6 server or by Shelf Manager[2] or other proxy
- Direct Ethernet LAN interface, where the Xilinx Zynq® UltraScale+™ PS Ethernet controller is dedicated to management traffic, not shared with the payload

Optional HPM.2 Serial over LAN (SoL)
- Uses HPM.2 IPMI over LAN facility to support Serial over LAN via a direct Ethernet connection
  - Payload SoL requires separate physical UART connection between payload and IPMC (alternatively, a Virtual UART can be used)
  - SoL for IPMC serial debug interface available, also
  - HPM.2 SOL extensions allow up to 15 concurrent SOL sessions, each with specific serial ports accessible to the IPMC, user chosen from up to 255 physical on-board serial ports
- Supplied open source ipmitool can be used as SoL client

Optional local System Event Log (SEL)
- Requires SEEPROM storage on board
- IPMI compliant System Event Log for events generated on the FRU(s) represented by the IPMC
- Can provide a useful historical record of events that have been recorded during operation of a board, perhaps for use in board diagnosis at a maintenance depot
- Events are also forwarded to Chassis Manager, as required by VITA 46.11

Optional support for persistent modifications to Sensor Data Records
- Non-volatile copy of SDR Repository can be configured in on-board SEEPROM
- Sensor threshold and hysteresis values can be configured dynamically via Pigeon Point extension commands, and are thereafter persistent across power cycles and resets of the board

Optional support for payload-controlled sensors
- Allows sensors that are implemented by the payload (e.g. an I^2C sensor connected to the payload CPU) but exposed by the IPMC as its own
- Covers discrete and threshold sensors

Optional support for persistent configuration parameters
- Parameters preserve values across IPMC power cycles and resets
- Used for most persistent data, such as serial port parameters, LAN and SoL parameters
- Framework for such treatment of other parameters, including those in custom firmware extensions

Simple, but powerful, firmware configuration mechanisms
- Configuration variables in a single config.h source file parameterize and determine inclusion/exclusion of subsystems during firmware image build
- Binary configuration files for FRU Information and Sensor Data Records (SDR) merged into firmware image
- FRU Information and SDR files produced from textual representations by special supplied compilers

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[2] The Pigeon Point Shelf Manager can be configured to assign IPv4 address parameters to LAN-attached IPMCs via HPM.3-defined mechanisms.

Numerous extensions beyond required IPMI/VITA 46.11/HPM.1 commands and functionality

- Warm Reset
- Get Device GUID
- Set BMC Global Enables
- Reset Watchdog Timer
- Set Watchdog Timer
- Get Watchdog Timer
- Get BMC Global Enables
- Clear Message Flags
- Get Message Flags
- Get Message
- Send Message
- Get System GUID
- Set User Name
- Get/Set Sensor Hysteresis
- Get/Set Sensor Thresholds
- Get/Set Sensor Event Enable
- Re-arm Sensor Events
- Get Sensor Event Status
- Get Sensor Type
- Activate/Deactivate Payload
- Suspend/Resume Payload Encryption
- Get Payload Activation Status
- Get Payload Instance Info
- Get/Set User Payload Access
- Get Channel Payload Support
- Get Channel Payload Version
- Get Channel OEM Payload Info Command
- Get/Set SOL Configuration Parameters
- FRU Control
  - Graceful Reboot and Issue Diagnostic Interrupt options
- Get FRU LED Properties
- Get LED Color Capabilities
- Get/Set FRU LED State
  - Lamp Test function
- Set FRU Activation
- Get FAN Speed Properties
- Get/Set Fan Level
- Get IPMB Link Info
- Get/Set FRU Persistent Control
- FRU Persistent Control Capabilities
- Get Power Supply Capabilities
- Get/Set Power Supply Status
- Abort Firmware Upgrade
- Query Self-test Results
- Query Rollback Status
- Initiate Manual Rollback

The following VITA 46.11-2022 commands are only supported with a Pigeon Point Tier-3 IPMC:

- Get/Set Command Enables
- Get/Set Configurable Command Sub-function Enables
- Get NetFn Support
- Get OEM NetFn IANA Support
- Get FRU Hash
- Get Payload Mode Capabilities
- Set Payload Mode
- Get Write Protect Capabilities
- Get/Set Write Protect Enables
- Get Control Bits Capabilities
- Get/Set Control Bits
- Get/Set Bridged Command Enables
- Get/Set Bridged Command Sub-function Enables
- Get Bridged NetFn Support
- Get/Set Bridged NetFn Policy

Rich set of Pigeon Point extension commands

- All extension commands implemented as IPMI-compliant OEM messages
- Get Status
- Get/Set Serial Interface Properties
- Get/Set Debug Level
- Get/Set Hardware Address
- Get/Set Payload Communication Timeout
- Disable/Enable Payload Control
- Reset IPMC
- Hang IPMC[3]
- Graceful Reset
- Diagnostic Interrupt Results
- Get/Set Payload Shutdown Timeout
- Get/Set Local FRU LED State
- Update Discrete Sensor
- Update Threshold Sensor
- Set EEPROM SDR Data
- Set EEPROM SDR Hysteresis
- Set EEPROM SDR Thresholds
- Reset EEPROM SDR Repository
- Get/Set GPIO Signal State
- Reset Non-Volatile Parameters and Reboot
- Get/Set FRU Info Write-Protect State

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[3] This function is used to test the IPMC watchdog.